Square pulse linear transformer driver

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(Received 13 December 2011; published 3 April 2012)

The linear transformer driver (LTD) technological approach can result in relatively compact devices that can deliver fast, high current, and high-voltage pulses straight out of the LTD cavity without any complicated pulse forming and pulse compression network. Through multistage inductively insulated voltage adders, the output pulse, increased in voltage amplitude, can be applied directly to the load. The usual LTD architecture [A. A. Kim, M. G. Mazarakis, V. A. Sinebryukhov, B. M. Kovalchuk, V. A. Vizir, S. N Volkov, F. Bayol, A. N. Bastrikov, V. G. Durakov, S. V. Frolov, V. M. Alexeenko, D. H. McDaniel, W. E. Fowler, K. LeCheen, C. Olson, W. A. Stygar, K. W. Struve, J. Porter, and R. M. Gilgenbach, Phys. Rev. ST Accel. Beams **12**, 050402 (2009); M. G. Mazarakis, W. E. Fowler, A. A. Kim, V. A. Sinebryukhov, S. T. Rogowski, R. A. Sharpe, D. H. McDaniel, C. L. Olson, J. L. Porter, K. W. Struve, W. A. Stygar, and J. R. Woodworth, Phys. Rev. ST Accel. Beams **12**, 050401 (2009)] provides sine shaped output pulses that may not be well suited for some applications like z-pinch drivers, flash radiography, high power microwaves, etc. A more suitable power pulse would have a flat or trapezoidal (rising or falling) top. In this paper, we present the design and first test results of an LTD cavity that generates such a type of output pulse by including within its circular array a number of third harmonic bricks in addition to the main bricks. A voltage adder made out of a square pulse cavity linear array will produce the same shape output pulses provided that the timing of each cavity is synchronized with the propagation of the electromagnetic pulse.

DOI: 10.1103/PhysRevSTAB.15.040401 PACS numbers: 84.70.+p, 84.60.Ve

I. INTRODUCTION

The linear transformer driver (LTD) [1,2] is a new method for constructing high current, high-voltage pulsed accelerators. The salient feature of the approach is switching and inductively adding the pulses at low voltage straight out of the capacitors through low inductance transfer and soft iron core isolation. LTD based drivers are considered for many applications including future very high current z-pinch inertial confinement fusion drivers like ZX, z-pinch inertial fusion energy drivers, and x-ray radiography. High currents can be achieved by feeding each core with many capacitors connected in parallel in a circular array. High voltage is obtained by inductively adding many stages in series. In addition to the relative compactness, LTD has a number of very significant advantages compared to the Marx-and-water-line technologies [3].

Up to now the usual LTD cavity architecture provided sinusoidally shaped pulse outputs. The flexibility and applicability of the LTD drivers could be greatly enhanced if we could change the output pulse shape according to the requirements of the various applications. For instance, the radiographic accelerators would be greatly benefited if the voltage applied to the x-ray diode had a square or even flattop shape. The square pulse LTD cavity described, built, and analyzed in this paper accomplishes exactly that.

The idea of the square pulse LTD is based on the Fourier theorem, which states that any waveform can be reproduced by the superposition of a series of sine and cosine waves. In particular, the constant function $f(x)$ for $0 \leq x \leq \pi$, defined as

$$f(x) = \frac{\pi}{4}, \tag{1}$$

can be reproduced as follows:

$$f(x) = \sum_{p=1}^{p_{\max}} \frac{\sin(2p-1)x}{2p-1}, \tag{2}$$

where $p_{\max} = \infty$. Figure 1 demonstrates the difference between Eqs. (1) and (2) depending on $p_{\max}$.

For $p_{\max} = 2$, Eq. (2) can be represented in the form

$$f_2(x) = \sin x + \frac{1}{a}\sin 3x, \tag{3}$$

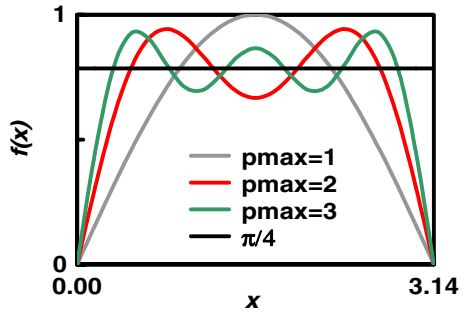

FIG. 1. The functions $f(x)$ given by Eq. (2) for $p_{\max} = 1$ to 3 compared with $f(x) = \pi/4$.

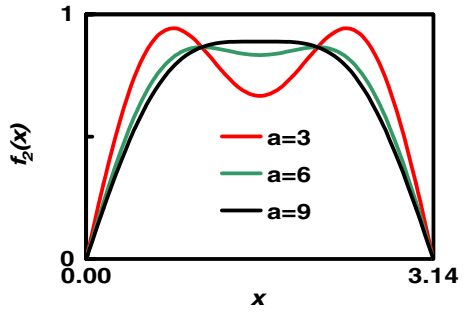

FIG. 2. The function $f_2(x)$ at $a = 3, 6, 9$.

where $a = 3$. If a in Eq. (3) increases from 3 to ~9, the top of the pulse flattens, as is shown in Fig. 2.

If the function $f_2(x)$ is the current in the load, in order to produce this current pulse the driving circuit has to deliver to the load two sine pulses with different frequencies, ω_1 and $\omega_2 \sim 3\omega_1$. The amplitude of the current pulse with the frequency ω_2 must be less than the one with the frequency ω_1. The LTD architecture [1,2] is convenient for this kind of pulse shaping because its discharge circuit is composed of multiple separate bricks connected in parallel. The output LTD pulse can have a flattop as in Fig. 2 if the bricks in the cavity are of two different kinds: a number of them are the standard "ω_1" bricks that deliver the main sinusoidal pulse into the load, and the others are the modified "ω_2" bricks that flatten the top of the output pulse.

In Sec. II we present brief analysis of the principles on which is based the selection of the square pulse LTD structure. Section III describes the design of the first square pulse LTD which was build and tested for this work. The simulation procedure is explained in Sec. IV, whereas Sec. V presents the experimental results compared with numerical simulations.

II. ESTIMATION OF THE SQUARE PULSE LTD PARAMETERS

The simplified electrical circuit of the square pulse LTD is shown in Fig. 3. It consists of s standard and m modified bricks. Each brick includes two capacitors charged in

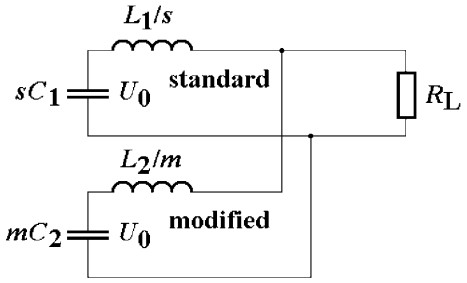

FIG. 3. Simplified electrical circuit of the square pulse LTD.

opposite polarity and connected in series with the switch. The two buses (metal plates) connect the capacitors with the load. In Fig. 3, C_1 and L_1 are, respectively, the total capacitance and inductance of the standard brick that generates the current pulse with the frequency ω_1. Similarly C_2 and L_2 denote the same parameters of the modified brick generating the current pulse with the frequency $\omega_2 \sim 3\omega_1$. All bricks are connected in parallel and triggered simultaneously at $t = 0$. The load resistance is R_L. We assume that both standard and modified bricks are charged to the same charge voltage U_0, as this is preferable in an actual cavity.

For an arbitrary set of the parameters, the equations describing the circuit of Fig. 3 cannot be solved analytically. Fortunately, for our purposes, the approximate solution to these equations, derived by taking into account a number of simplifying assumptions, can adequately describe the above circuit behavior. These assumptions are: (i) since the standard bricks store the main energy, they should be matched to the cavity load, i.e., the following condition must be satisfied:

$$\sqrt{\frac{L_1/s}{sC_1}} = \frac{1}{s}\sqrt{\frac{L_1}{C_1}} = \frac{1}{s}\rho_1 \sim R_{\mathrm{L}}, \tag{4}$$

where $\rho_1 = \sqrt{\frac{L_1}{C_1}}$ is the circuit impedance of the standard brick. (ii) To flatten the output pulse top, the circuit frequency of the modified brick must be ~3 times that of the standard brick, resulting in

$$\sqrt{L_1 C_1} \sim 3\sqrt{L_2 C_2}. \tag{5}$$

(iii) In the standard fast LTDs, the bricks are designed in such a way that for a given capacitor and switch the inductance L_1 is reduced to its minimum possible value. This means that the inductance L_2 is limited, at least from below, by the value

$$L_2 \sim L_1. \tag{6}$$

Equation (4) approximates the matched load of the square pulse LTD, whereas Eqs. (5) and (6) give the estimate for the capacitance of the modified brick as a function of the capacitance of the standard brick

$$C_2 \sim \tfrac{1}{9} C_1. \tag{7}$$

Simulations show that if the conditions (4)–(6) are satisfied, the standard and modified bricks discharge into the load R_L as if they were almost independent of each other. Then the amplitude of the current delivered by s standard bricks into the *matched* load R_L is

$$I_1 \sim 0.5 \frac{U_0}{\rho_1} s. \tag{8}$$

The amplitude of the current I_2 delivered by the $m(<s)$ modified bricks into the load $R_L \sim \frac{\rho_1}{s} \sim \frac{m}{3s} \frac{\rho_2}{m} < 0.33 \frac{\rho_2}{m}$, is

$$I_2 \sim 0.9 \frac{U_0}{\rho_2} m. \tag{9}$$

This is because the load that the modified bricks see, R_L, is much smaller (under matched) than their characteristic impedance $\rho_2 = \sqrt{\frac{L_2}{C_2}}$.

Equations (5)–(9) indicate that the shape of the load pulse [defined by the coefficient a in Eq. (3), see Fig. 2] depends on the ratio of the number of standard and modified bricks in the cavity, because

$$a = \frac{I_1}{I_2} \sim 0.55 \frac{\rho_2}{\rho_1} \frac{s}{m} \sim 1.65 \frac{s}{m}. \tag{10}$$

III. DESIGN AND DIAGNOSTICS OF THE SQUARE PULSE LTD

The square pulse LTD was designed containing $s = 4$ standard bricks each consisting of two capacitors GA 35460 (100 kV, 8 nF) connected in series, and $m = 2$ modified bricks each consisting of four TDK ceramic capacitors type UHV-12A (50 kV, 1.7 nF) connected in series. The layout of this cavity is presented in Fig. 4, showing the bottom row of the capacitors in the bricks. In the tests described below, the number of standard bricks was varied in order to compare the results with simulations.

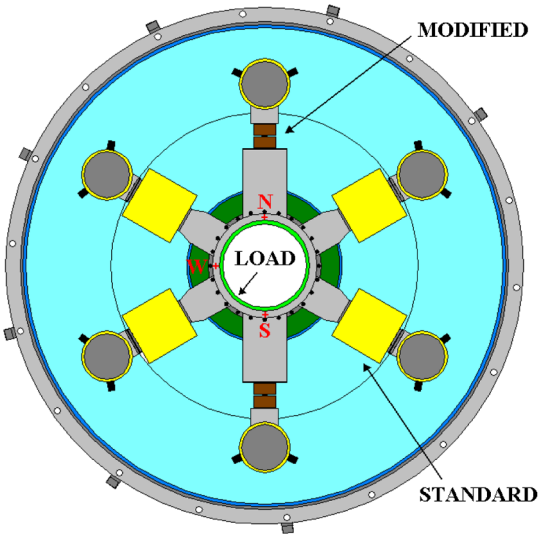

FIG. 4. Square pulse LTD with 4 standard and 2 modified bricks. The outer diameter of the cavity is 140 cm. The location of the cavity core is indicated in dark green.

Figure 5 shows the design of the modified and standard bricks of the cavity. In both types of bricks the same multigap switches with corona discharge [4,5] are used allowing these bricks to fire simultaneously when their capacitors are charged to the same voltage.

The cavity core is made of ET3425 iron tape with the thickness $\delta = 80$ μm, and the length of its center line [6] (here is equal to the length of the core mean circumference) is $\ell \sim 1.2$ m. It consists of 6 rings, the total cross section of iron in these rings being $S \sim 53$ cm^2. At passive premagnetization [6], which was used in tests described below, the volt-second integral of this core is $VS_{\mathrm{CORE}} \sim 17$ mV s.

The cavity load is made as a 10-mm-wide, 124-mm-long double walled cylindrical cavity filled with KBr water solution; the position of this cavity is shown in Fig. 4 in light green. The load voltage U_L was measured by using an external oil-filled resistive voltage divider. The input of this divider was located in the center of the cavity load, measuring the average load voltage around the load circumference.

The current flowing in the load was measured by using 3 differential-output B-dot monitors similar to those described in [7]. Red crosses in Fig. 4 marked as N, W, and S indicate the location of these monitors relative to the position of the modified bricks in the cavity. The resistance of the load was defined as $R_L = U_L/I_L$, where U_L is the load voltage measured by the external voltage divider, and I_L is the load current calculated as

$$I_L = 0.5 I_W + 0.25 I_N + 0.25 I_S, \tag{11}$$

where I_W, I_N, and I_S are integrated signals from the corresponding B-dot probes. Equation (11) assumes that the current between the two right standard bricks is the same as that between the two left standard bricks.

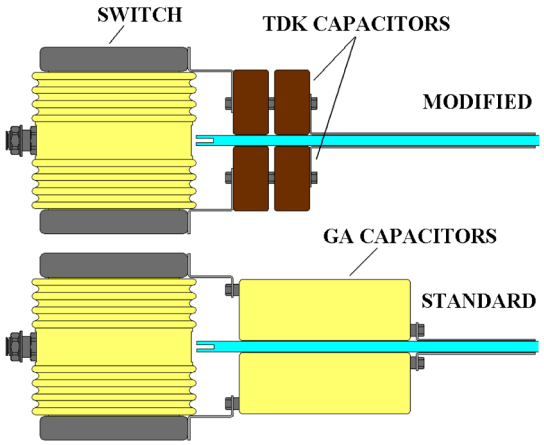

FIG. 5. Modified brick with TDK ceramic capacitors and standard brick with GA 35460 oil-filled capacitors.

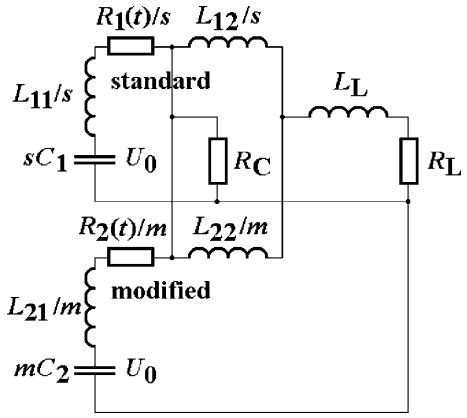

FIG. 6. Square pulse LTD circuit used in PSPICE simulations.

IV. SIMULATION

The behavior of the square pulse LTD was simulated in PSPICE[1] [8] by using the circuit presented in Fig. 6. It includes $s = 4$ standard and $m = 2$ modified bricks. The capacitors C_1 and C_2 have capacitance equal, respectively, to the total capacitance of the standard and modified brick, and they are charged to the same charge voltage U_0. The inductors L_{11} and L_{21} represent the inductance of the capacitors and the switches in the bricks, and L_{12} and L_{22} represent the inductance of the strip lines connecting the capacitors with the accelerating gap of the cavity. The load inductance is L_L, and its resistance is R_L.

Each of the resistors $R_1(t)$ and $R_2(t)$ consist of two parts connected in series, one of them represents the constant resistance of the capacitors and the other the current-dependent resistance of the gas switches [9]. The model of Ref. [9] was used to simulate the brick switch resistance in order to separately take into account the influence of the different currents flowing in the standard and modified bricks.

The resistance R_C connected in parallel to the inputs of the strip lines simulates the energy loss in the cavity core due to generation of the Eddy current in its material. According to [6], the value of this resistance is

$$R_C = 8\frac{\rho S}{\ell \delta^2}\frac{\Delta B}{\Delta B(\tau)}, \tag{12}$$

where $\rho = 5 \times 10^{-7}$ Ohm m is the specific resistivity of ET3425 iron, $\Delta B = 3.2$ T the induction swing of ET3425 iron at passive premagnetization, and

$$\Delta B(\tau) = \frac{1}{S}\int_0^\tau U(t)dt \tag{13}$$

the induction swing produced in the core by the τ-long voltage pulse $U(t)$ applied to the core. In terms of the volt-second integrals, Eq. (12) gets the form

$$R_C = 8\frac{\rho S}{\ell \delta^2}\frac{VS_{\mathrm{CORE}}}{VS_{\mathrm{PULSE}}} \sim \frac{46.75}{VS_{\mathrm{PULSE}}\ [\mathrm{mV\,s}]}\ \mathrm{Ohms}, \tag{14}$$

where VS_{PULSE} is the volt-second integral applied to the core (i.e. to the resistance R_C). This integral depends on the number of standard bricks s in the cavity and the load resistance R_L. For each given s and R_L, the values of VS_{PULSE} and R_C were defined in simulations by using the iteration process.

V. EXPERIMENTAL RESULTS

The parameters of the PSPICE circuit in Fig. 6 were verified in experiments where the cavity was charged to $U_{\mathrm{CH}} = \pm 100$ kV (corresponding to $U_0 = 200$ kV in Fig. 6) for different loads R_L, varying between 0.85 and 3.45 Ohm, without the modified bricks and without the top metal cover. The removal of this cover interrupts the current loop around the core, thus excluding any influence of the core on the discharge circuit of the LTD cavity. Figure 7 shows, as an example, the recorded and simulated load voltage at $s = 4$, $m = 0$, $R_L \sim 1.6$ Ohm, and $U_{\mathrm{CH}} = \pm 100$ kV. The PSPICE trace is obtained with $R_C = 10^6$ Ohms in the circuit of Fig. 6.

The installation of the modified bricks into the cavity squares the shape of the output pulse, as this is shown in Fig. 8, where the recorded and simulated load voltage traces for $s = 4$, $m = 2$, $R_L \sim 1.6$ Ohm, and $U_{\mathrm{CH}} = \pm 100$ kV are plotted. This shot was made also without the core and was simulated with $R_C = 10^6$ Ohms in the circuit of Fig. 6.

The top of this pulse at $s/m = 2$ is almost flat; this means that Eq. (10) must be modified:

$$a \sim 3\frac{s}{m}. \tag{15}$$

The need for such modification appears because of relatively high resistance of the TDK ceramic capacitors, which was measured to be ~0.3 Ohms per capacitor

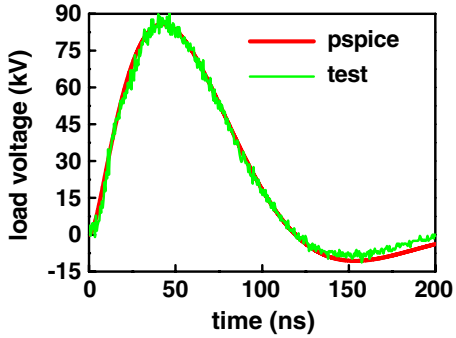

FIG. 7. The recorded and simulated load voltage in a shot without the current loop around the core and without the modified bricks, at $s = 4$, $m = 0$, $R_L \sim 1.6$ Ohms, and $U_{\mathrm{CH}} = \pm 100$ kV. The currents I_W, I_N, and I_S recorded in shots without the modified bricks at each given R_L were equal within $\pm 5\%$.

[1]PSPICE is a registered trademark of MicroSim Corporation.

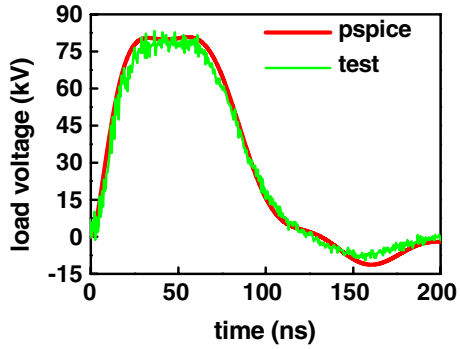

FIG. 8. The recorded and simulated load voltage in a shot without of the current loop around the core, at $s = 4$, $m = 2$, $R_L \sim 1.6$ Ohms, and $U_{CH} = \pm 100$ kV.

(resulting in ~1.2 Ohms per each modified brick). This resistance damps the amplitude of the second current peak produced in the load by the modified bricks.

Figure 9 shows the simulated voltage trace across the capacitors of the modified bricks in this shot. The peak reversal voltage is ~36 kV, which is ~18% of the charge voltage.

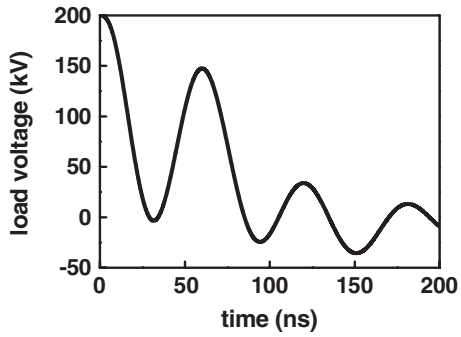

FIG. 9. Simulated voltage across the capacitors in the modified bricks. Same shot as in Fig. 8.

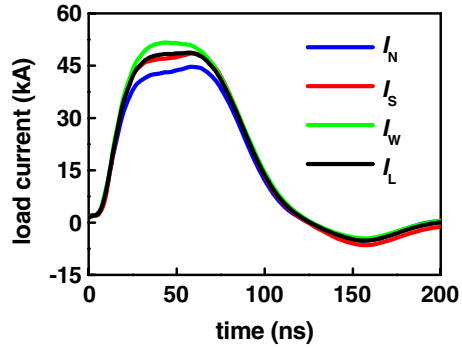

FIG. 10. Load current measured by separate B-dot probes, and total load current I_L calculated by using Eq. (11). Same shot as in Fig. 8.

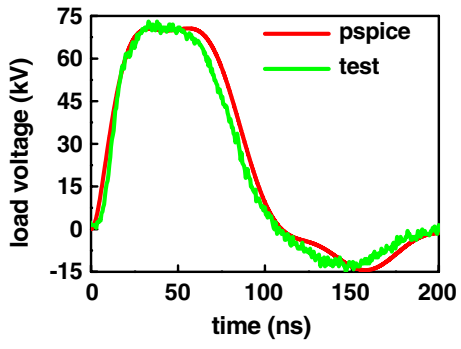

FIG. 11. Recorded and simulated load voltage in a shot with the core, at $s = 4$, $m = 2$, $R_L \sim 1.6$ Ohm, and $U_{CH} = \pm 100$ kV. Compared with Fig. 8, the installation of the core reduces the voltage amplitude from ~77 kV to ~70 kV because of energy loss in the core.

Figure 10 presents the total load current I_L calculated by using Eq. (11) in comparison with the currents measured in this shot by separate B-dot probes. The current I_W measured between the standard bricks is larger than I_N and I_S measured opposite the modified bricks, indicating that the current flow in our circular load cavity is not homogeneous.

The installation of the core reduces the load voltage amplitude (Fig. 11), indicating an energy loss associated with the core. Figure 11 shows the load voltage trace recorded with the same conditions as that in Fig. 8; the only difference between these two results is the presence of the top metal cover closing the current loop around the core and the installation of the core in the shot presented in Fig. 11. The voltage amplitude in Fig. 11 is ~10% less than that in Fig. 8, and the same reduction is observed in the PSPICE trace which was calculated with self-consistent values of $VS_{PULSE} = 5.2$ mV s and $R_C = 8.99$ Ohms [see Eq. (13)]. The energy loss (during the main pulse, before the voltage becomes negative) in $R_C = 8.99$ Ohms is ~35 J or ~10% of total energy stored in the capacitors

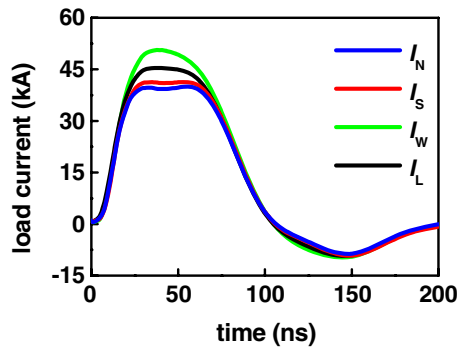

FIG. 12. Load current measured by separate B-dot probes, and total load current I_L calculated by using Eq. (11). Same shot as in Fig. 11.

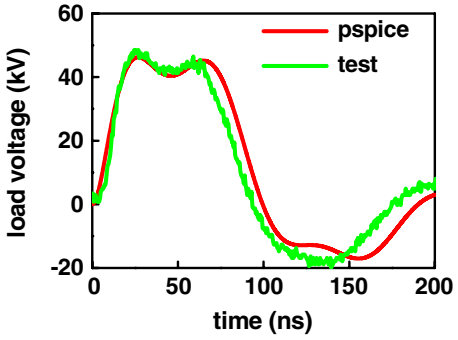

FIG. 13. Recorded and simulated load voltage at $s = m = 2$, $R_L \sim 1.6$ Ohms, and $U_{CH} = \pm 100$ kV. At reduced s/m the pulse becomes double peaked.

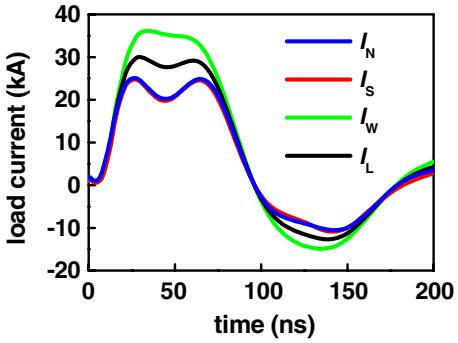

FIG. 14. Load current measured by separate B-dot probes, and total load current I_L calculated by using Eq. (11). Same shot as in Fig. 13.

at ± 100 kV charge voltage. Figure 12 shows the currents recorded in this shot.

In order to check if the relative number of the modified bricks determines the shape of the output pulse as described above in Sec. II, the performance of the square pulse LTD was tested with $s = 2$ standard and $m = 2$ modified bricks (with the core). Figure 13 presents the recorded and simulated ($VS_{\mathrm{PULSE}} = 3.34$ mV s, $R_C = 14$ Ohms) load voltage in this case, indicating that the pulse becomes double peaked, as expected. The load currents recorded in this shot are shown in Fig. 14.

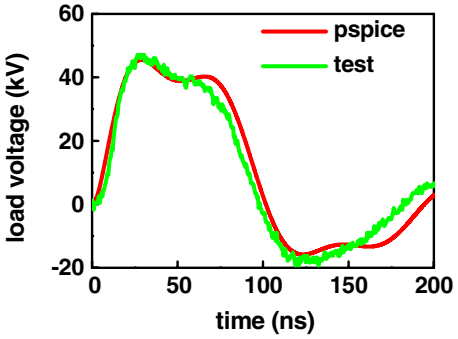

FIG. 15. Recorded and simulated load voltage at $s = m = 2$, $R_L \sim 1.6$ Ohms, and $U_{CH} = \pm 100$ kV. The increase of the inductance of the modified bricks causes the top of the pulse to decrease much faster (compare with the traces in Fig. 13).

Simulations predict that the top of the output pulse may rise or fall depending on the inductance of the modified bricks. This is because at the given load resistance this inductance determines the amplitude of the second current peak produced by the modified bricks in the load. In order to check this prediction in experiments, the width of the output strip lines of the modified bricks was reduced from 120 to 55 mm, thus increasing their inductance by $\sim$30 nH. Figure 15 presents the recorded and simulated ($VS_{\mathrm{PULSE}} = 3.22$ mV s, $R_C = 14.5$ Ohms) load voltage in this case; the top of the output pulse decreases much faster, as predicted.

VI. CONCLUSION

The shape of the output LTD pulse can become square instead of the regular sinusoidal if the cavity is assembled with a number of modified bricks with capacitors of $\sim$10 times less capacitance than the capacitors of the standard bricks. The ratio of the modified to standard bricks defines the shape of the output pulse.

The top of the output pulse can be made flat, and also it can be made rising or falling depending on the inductance of the modified bricks. This opens the way to generate the shaped output pulses which are most preferable for specific applications.

Experiments with square pulse LTD which included modified bricks with ceramic capacitors, indicate that Eq. (10) should be modified into Eq. (15). This is due to the larger resistance of the ceramic capacitors. The square pulse LTD would be more efficient if low resistance oil-filled capacitors were used in both standard and modified bricks.

Compared with the standard bricks, the modified bricks occupy approximately the same volume inside the cavity but store less energy. This means that specific energy stored in the square pulse LTD cavity is less than that in the standard one. This conclusion may increase the size of the cavities in order to keep the stored energy constant for certain applications that require a large amount of currents per cavity. Other constraints may be the $\sim$18% voltage reversal on the capacitors of the modified bricks that could reduce their lifetime.

Concluding, we would like to reemphasize the advantage of the square pulse LTD as compared to the standard one. It can produce a more suitable power pulse (flattop or trapezoidal) for a number of applications such as: z-pinch drivers, flash radiography, high power microwaves, etc. In this paper, we presented the design and first test results of an LTD cavity that generates such a type of output pulse by including within its circular array a number of third harmonic bricks in addition to the main bricks.

ACKNOWLEDGMENTS

The authors would like to thank Academician RAS B. M. Kovalchuk for the support of this work. Sandia is a multiprogram laboratory operated by Sandia Corporation, a Lockheed Martin Company, for the U.S. Department of Energy under Contract No. DE-AC04-94-AL85000.

[1] A. A. Kim, M. G. Mazarakis, V. A. Sinebryukhov, B. M. Kovalchuk, V. A. Vizir, S. N Volkov, F. Bayol, A. N. Bastrikov, V. G. Durakov, S. V. Frolov, V. M. Alexeenko, D. H. McDaniel, W. E. Fowler, K. LeCheen, C. Olson, W. A. Stygar, K. W. Struve, J. Porter, and R. M. Gilgenbach, Phys. Rev. ST Accel. Beams **12**, 050402 (2009).

[2] M. G. Mazarakis, W. E. Fowler, A. A. Kim, V. A. Sinebryukhov, S. T. Rogowski, R. A. Sharpe, D. H. McDaniel, C. L. Olson, J. L. Porter, K. W. Struve, W. A. Stygar, and J. R. Woodworth, Phys. Rev. ST Accel. Beams **12**, 050401 (2009).

[3] W. A. Stygar, M. E. Cuneo, D. I. Headley, H. C. Ives, R. J. Leeper, M. G. Mazarakis, C. L. Olson, J. L. Porter, T. C. Wagoner, and J. R. Woodworth, Phys. Rev. ST Accel. Beams **10**, 030401 (2007).

[4] A. A. Kim, B. M. Kovalchuk, A. N. Bastrikov, V. G. Durakov, S. N. Volkov, and V. A. Sinebryukhov, in *Proceedings of the 13th IEEE International Pulsed Power Conference*, edited by R. Reinoivsky and M. Newton (IEEE, Piscataway, NJ, 2001), p. 1491.

[5] J. R. Woodworth, J. A. Alexander, F. R. Gruner, W. A. Stygar, M. J. Harden, J. R. Blickem, G. J. Dension, F. E. White, L. M. Lucero, H. D. Anderson, L. F. Bennett, S. F. Glover, D. Van De Valde, and M. G. Mazarakis, Phys. Rev. ST Accel. Beams **12**, 060401 (2009).

[6] A. A. Kim, M. G. Mazarakis, V. I. Manylov, V. A. Vizir, and W. A. Stygar, Phys. Rev. ST Accel. Beams **13**, 070401 (2010).

[7] T. C. Wagoner, W. A. Stygar, H. C. Ives, T. L. Gilleland, R. B. Spielman, M. F. Johnson, P. G. Reynolds, J. K. Moore, R. L. Mourning, D. L. Fehl, K. E. Androlewicz, J. E. Bailey, R. S. Broyles, T. A. Dinwoodie, G. L. Donovan, M. E. Dudley, K. D. Hahn, A. A. Kim, J. R. Lee, R. J. Leeper, G. T. Leifeste, J. A. Melville, J. A. Mills, L. P. Mix, W. B. S. Moore, B. P. Peyton, J. L. Porter, G. A. Rochau, G. E. Rochau, M. E. Savage, J. F. Seamen, J. D. Serrano, A. W. Sharpe, R. W. Shoup, J. S. Slopek, C. S. Speas, K. W. Struve, D. M. Van De Valde, and R. M. Woodring, Phys. Rev. ST Accel. Beams **11**, 100401 (2008).

[8] MicroSim Schematics, Version 6.1b—November 1994. MicroSim Corporation, 20 Fairbanks, Irvine, California 92718, USA.

[9] A. A. Kim, V. G. Durakov, S. N. Volkov, A. N. Bastrikov, B. M. Kovalchuk, V. A. Synebryukhov, C. V. Frolov, V. M. Alexeenko, L. Veron, M. Toury, C. Vermare, R. Nicolas, F. Bayol, and C. Drouilly, in *Proceedings of the 14th Symposium on High Current Electronics*, edited by B. Kovalchuk and G. Remnev (Institute of High Current Electronics SD RAS, Tomsk, Russia, 2006), p. 297.